The status of wafer probing for PHENIX silicon pixel tracker

9 December 2004

RIKEN
Kohei Fujiwara, Johann.M.Heuser, Tatsuya Iwabuti

1. Introduction

☆ The PHENIX silicon pixel tracker consits of 2 cylindlical layers.

- 1st layer:10 staves
- 2nd layer:20 staves

↓

Number of necessary ladders are 120 ladders in total.

↓

Number of necessary ALICE1LHCb readout chips are 480 chips.

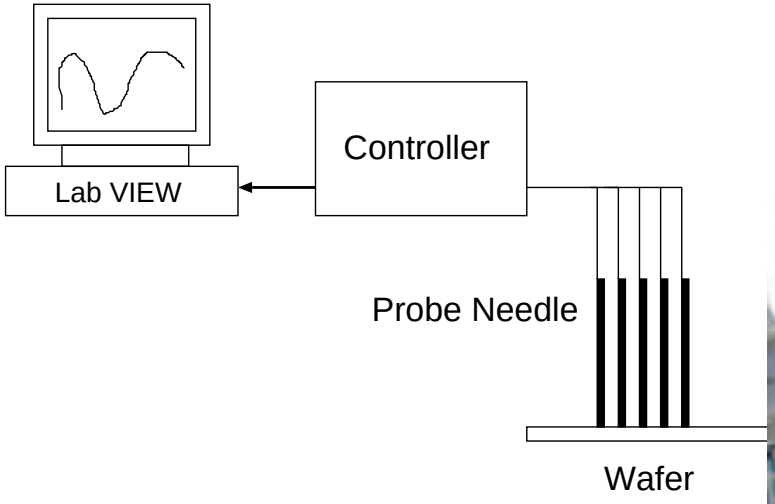
☆ We aim at obtaining 480 readout chips+spares(∼600 chips).

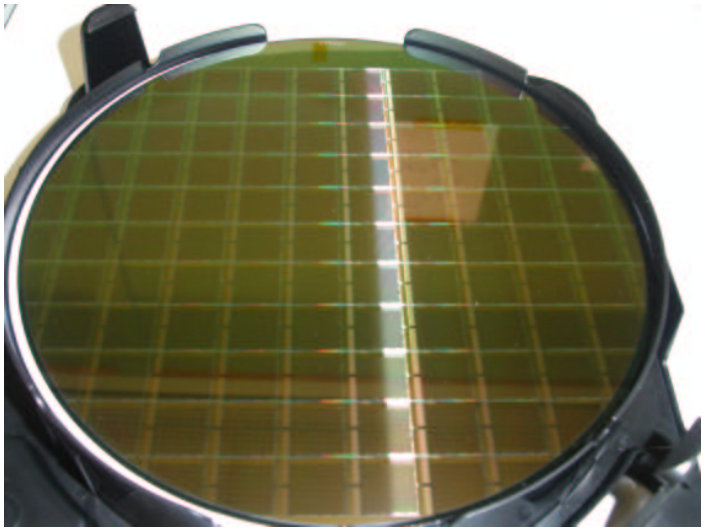
- We have probed 13 out of 16 wafers(1118 chips).
- 14th wafer is under probing.
- We have 374 chips for ladders.

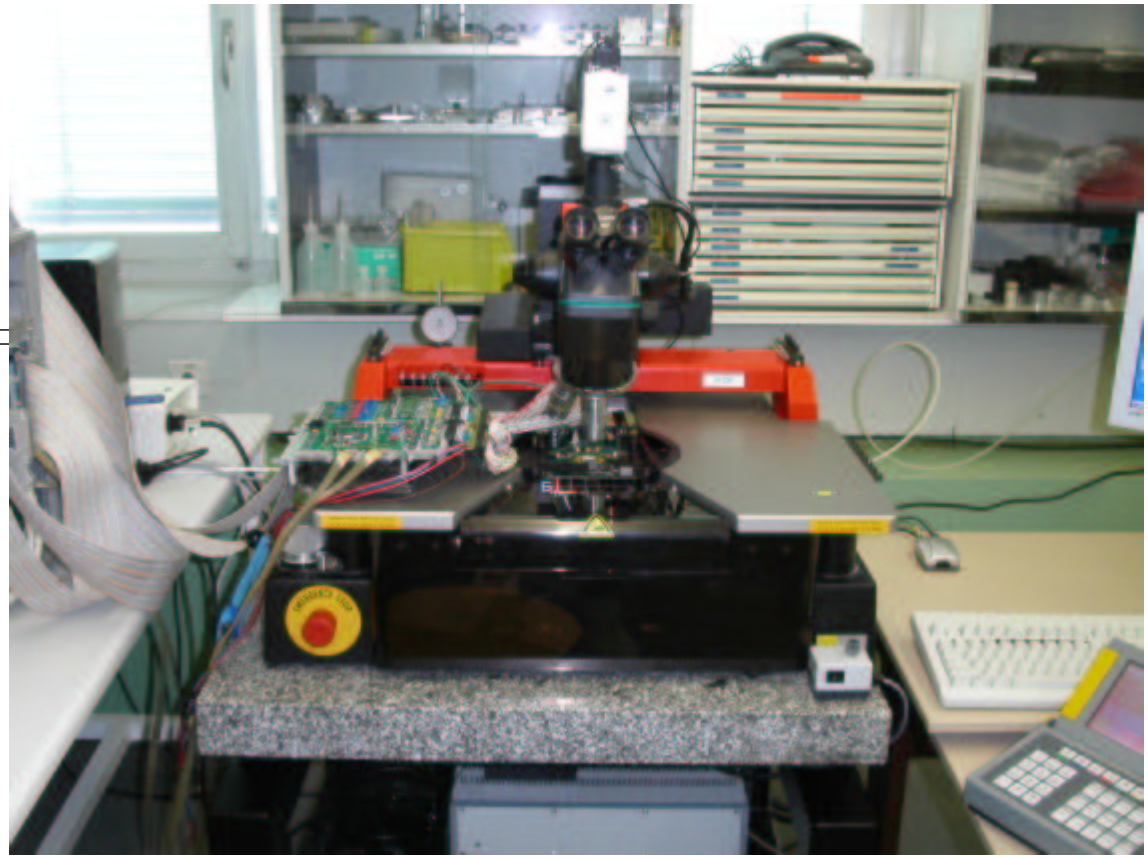
2. Wafer probing

☆ ALICE1LHCb readout chips are probed on the semi automatic prober in wafer level.

☆ One wafer contains 86 readout chips.







Classification

- The test system is constructed by NI LabView and ROOT.
- Readout chips are classified into 3 classes.

The item of common test

- JTAG and DAC functionality for chip control.
- Current for analog circuit < 350mA.
- Current for digital circuit < 270mA.
- No noisy pixels.
- Normal digital output.
- Existence of a threshold.

↓Passed ↓Failed

Classification for Class 1 or Class 2

- Number of dead pixels $< 1\%$(82 pixels).
- Minimum threhsold < 30mV($1980e^{-}$).

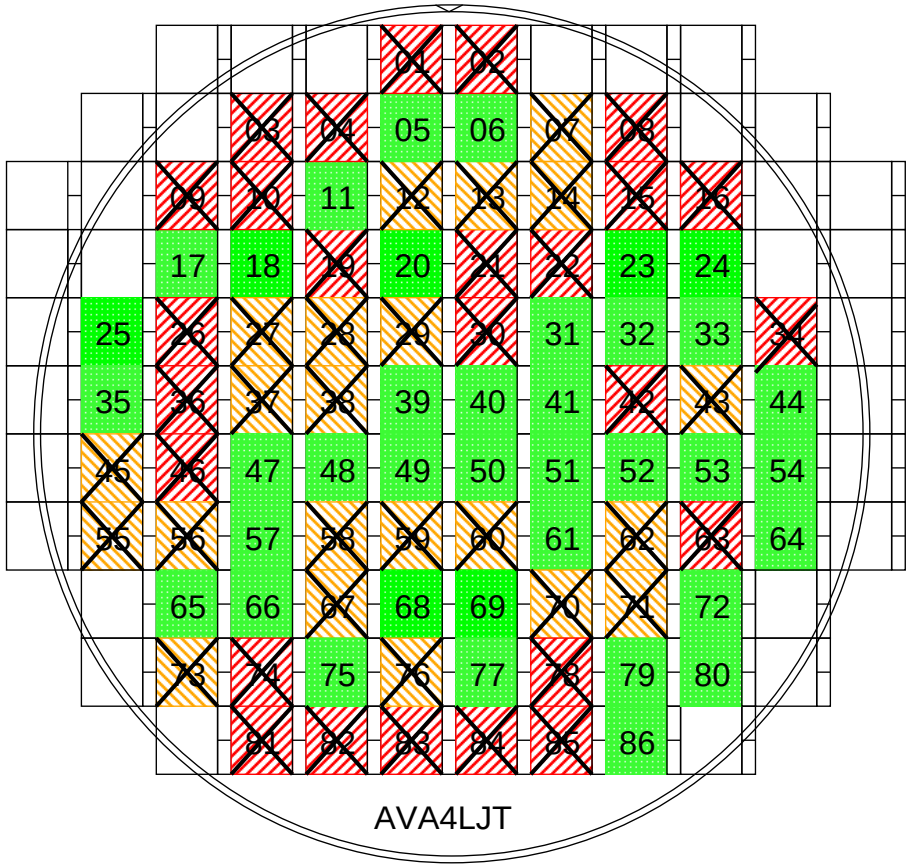
Class 3

↓Passed ↓Failed

Class 1 Class 2

3. Result of probing

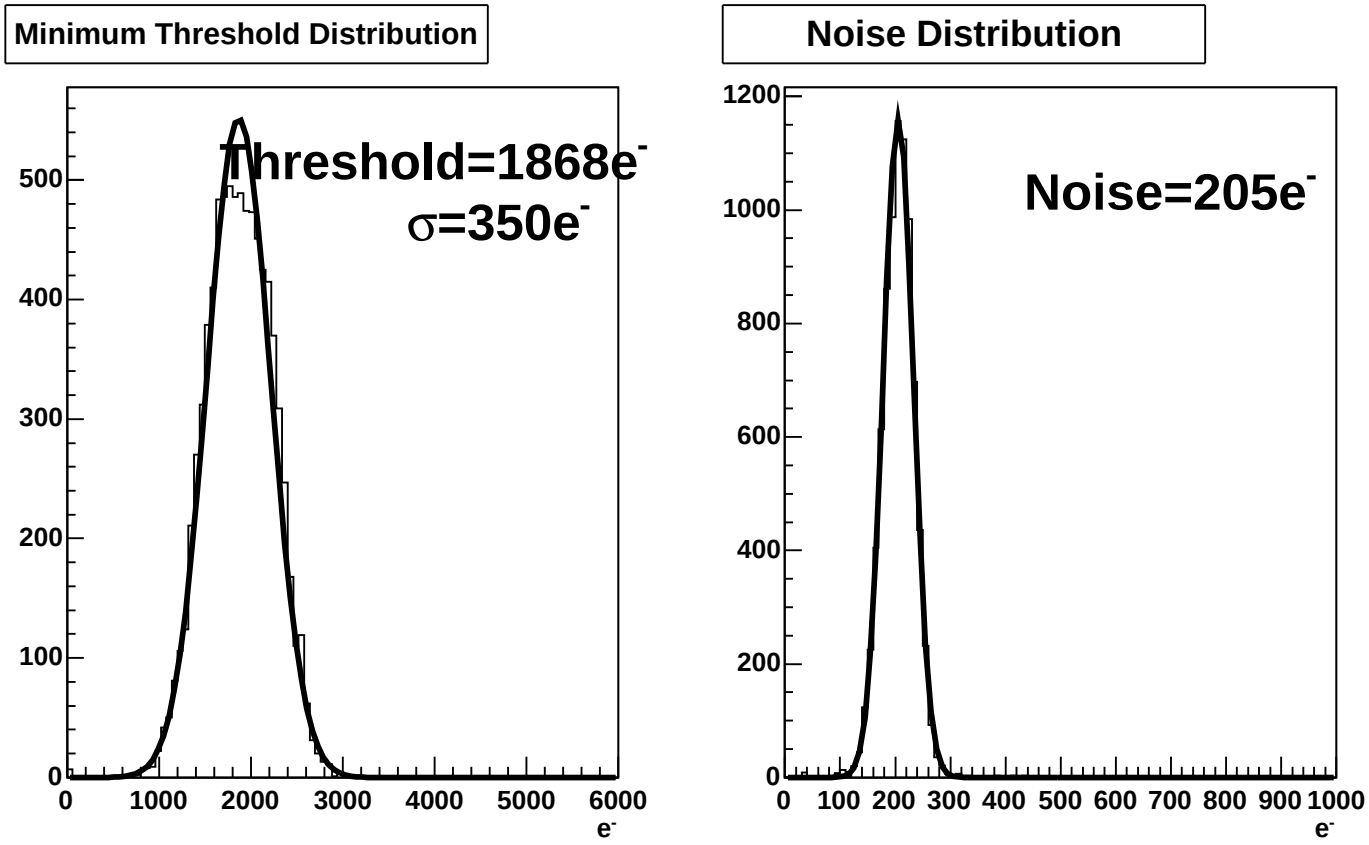
- A typical wafer map(4th:AVA4LJT)



Class 1	37%
Class 2	16%
Class 3	47%

- ☆ 38 Class 1 chips are on the wafer.
- ☆ Class 1 chips are mainly in the center of a wafer.

- Minimum threshold distribution and noise distribution on a chip



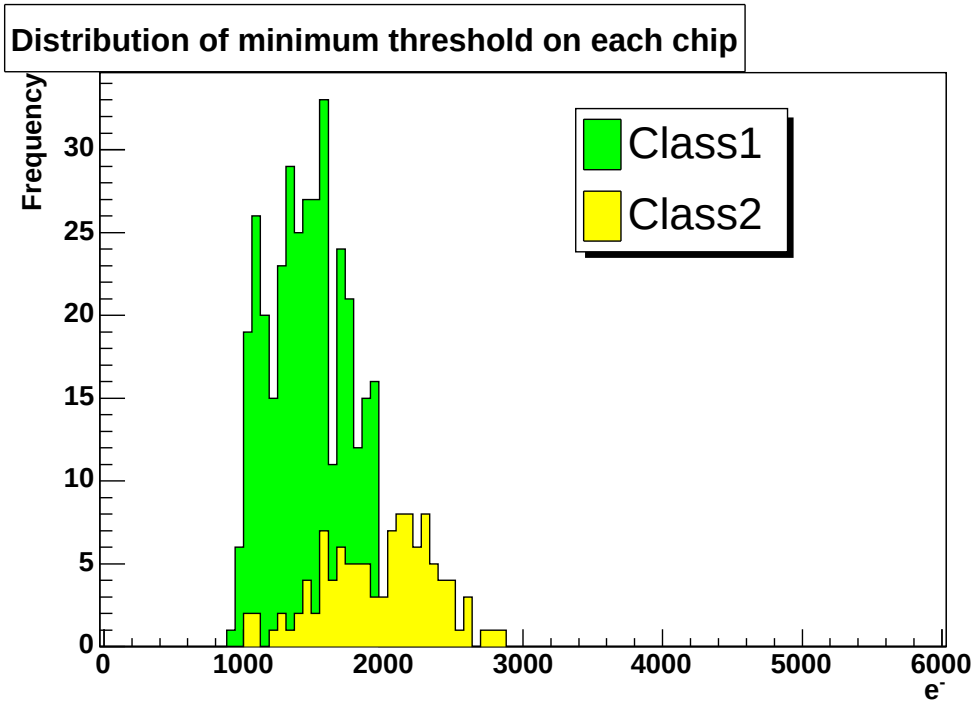
☆ The minimum threshold is 1868e$^-$.

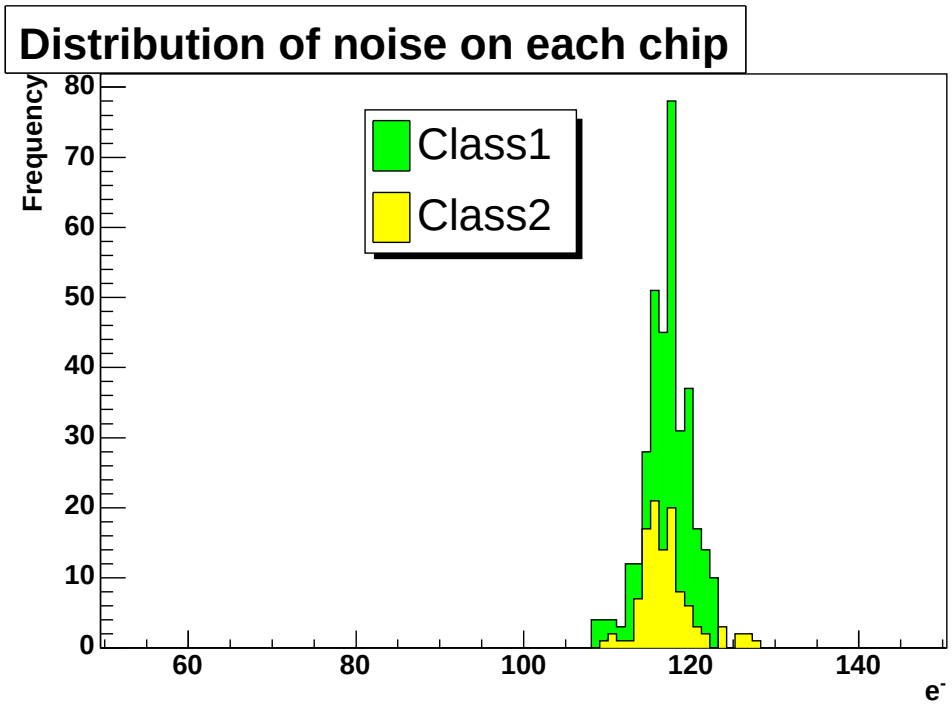
☆ Usually a thickness of 200μm silicon sensor by the MIP is around 22000e$^-$.

↓

The signal to the noise ratio is more than 10 on the ALICE1LHCb readout chip.

- Minimum threshold and noise distribution for all Class 1 and Class 2 chips





☆ The range of minimum threshold on each Class 1 chip is wide.

4. Occured problems

☆ From 9th wafer we have some problems.

◆ We get the yeild rate as the following.

Class 1	31.3%	374 chips
Class 2	10.1%	120 chips
Class 3	57.6%	698 chips

◆ Wafer 9th, 10th, 11th, 12th, 13th and 14th have problems.

→ At present the yeild rate is going down.

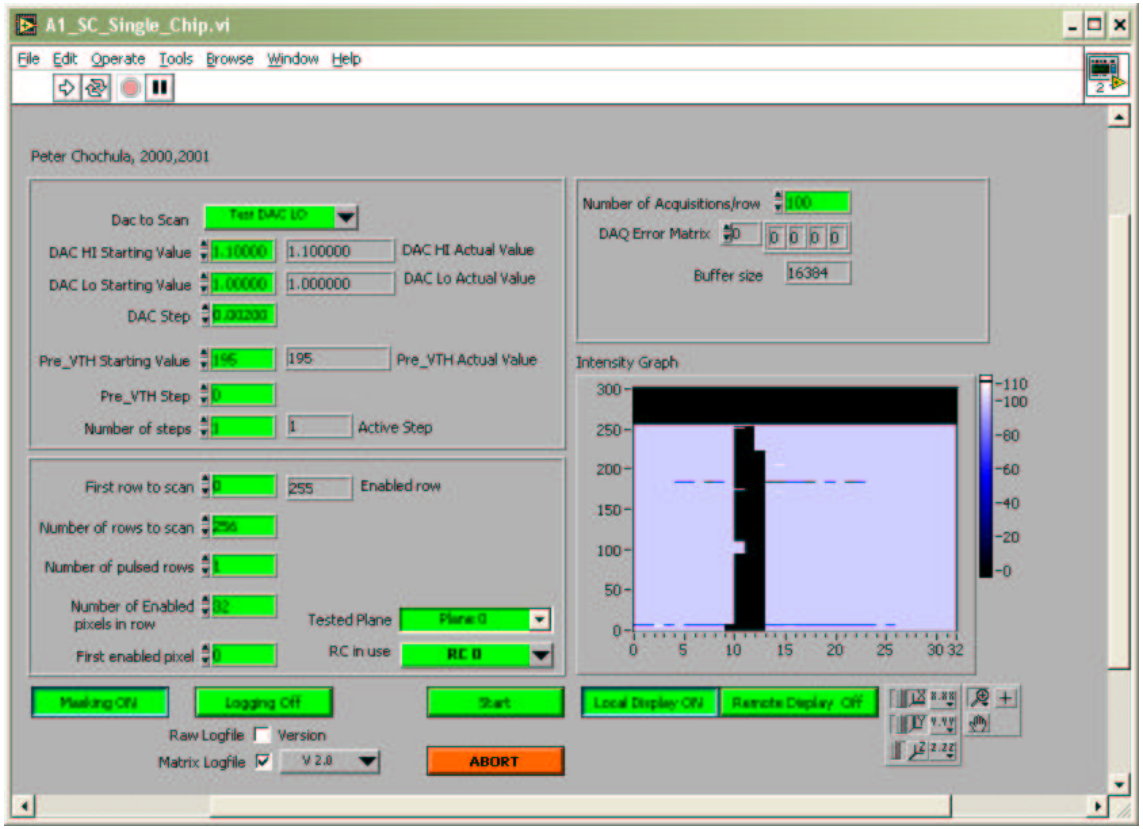
	Wafer Name	Class 1	Class 2	Class 3		Wafer Name	Class 1	Class 2	Class 3
1	ABA4J4T	46.5%	4.6%	48.8%	8	AZA4IZT	25.6%	4.7%	70.9%
2	AAA4J5T	37.2%	2.3%	60.4%	9	ATA4I5T	43.0%	3.5%	5.3%
3	A9A4J6T	29.1%	9.3%	61.6%	10	AZA4E1T	19.8%	2.3%	77.9%
4	AVA4LJT	44.2%	29.1%	26.7%	11	ACA4J3T	0.0%	1.2%	98.8%
5	ATA4LLT	27.9%	32.6%	39.5%	12	AQA4DTT	24.4%	1.2%	74.4%
6	A3A4JCT	40.7%	15.1%	44.2%	13	A9A4ERT	30.2%	2.3%	67.5%
7	AXA4LHT	38.4%	22.1%	39.5%	14	AWA4E4T	32.9%	11.0%	56.1%

Main problems

☆ JTAG functionality test error around column 12.

☆ Missing clolumns around column 12.

→ ATA4I5T(9th), AZA4E1T(10th), AQA4DTT(12th), A9A4ERT(13th), AWA4E4T(14th)



☆ About wafer ACA4J3T(11th), 60 out of 86 chips draw 2 times more current.

Problem chips

☆ At the moment we have 77 problem chips in total.

Wafer name	Problem chips
ATA4I5T(9th)	23/86
AZA4E1T(10th)	26/86
AQA4DTT(12th)	22/86
A9A4ERT(13th)	3/86
AWA4E4T(14th)	3/86

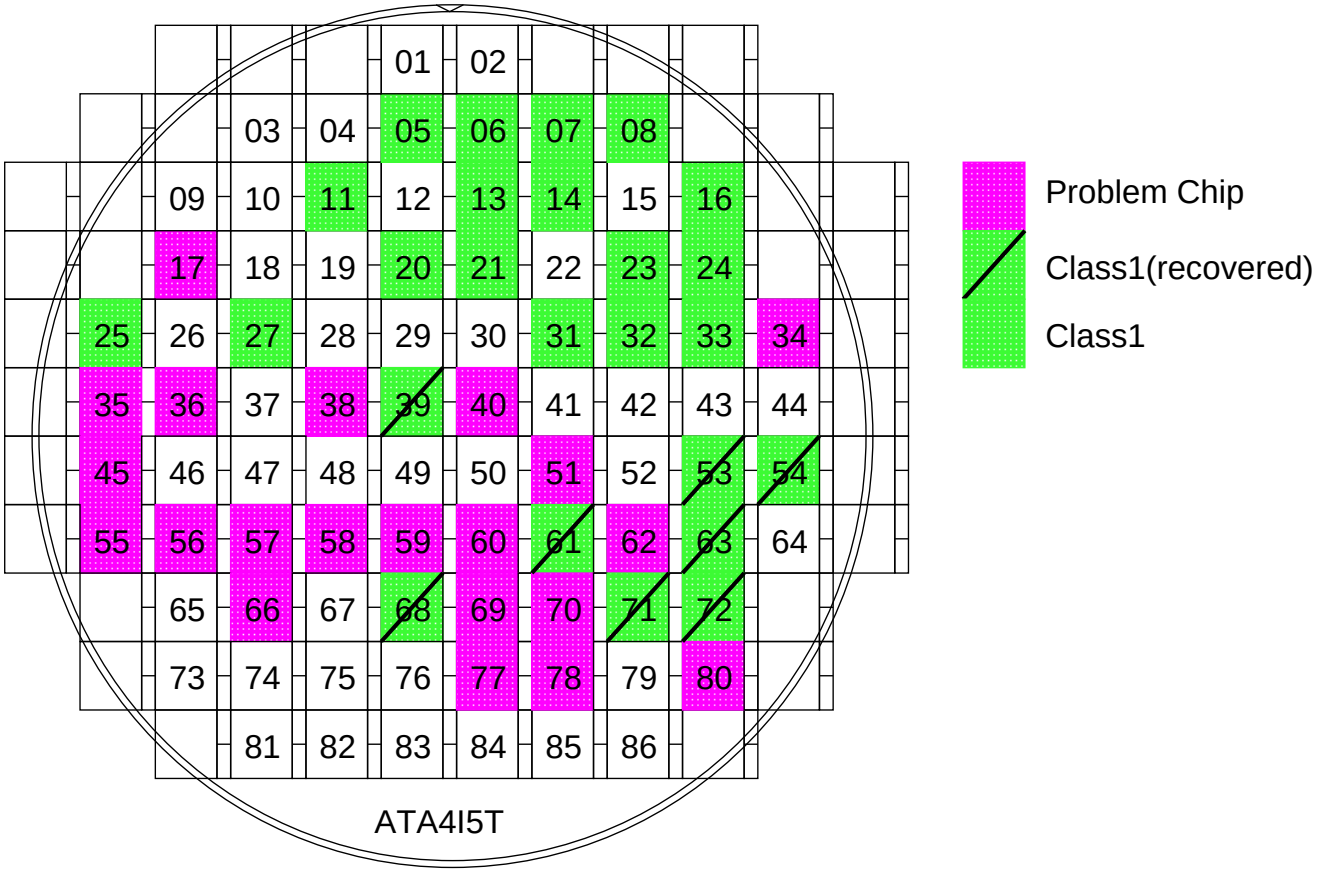
☆ We could recover these chips by increasing Vdd_Analog which is applied to analog circuit.

→ JTAG functionality test error and missing columns were recovered.

☆ Then 29 chips became Class1 in total.

Wafer name	Recovered chips	Recovered / Problem
ATA4I5T	8	26.7%
AZA4E1T	7	26.9%
AQA4DTT	11	50.0%
A9A4ERT	2	66.7%
AWA4E4T	1	33.3%

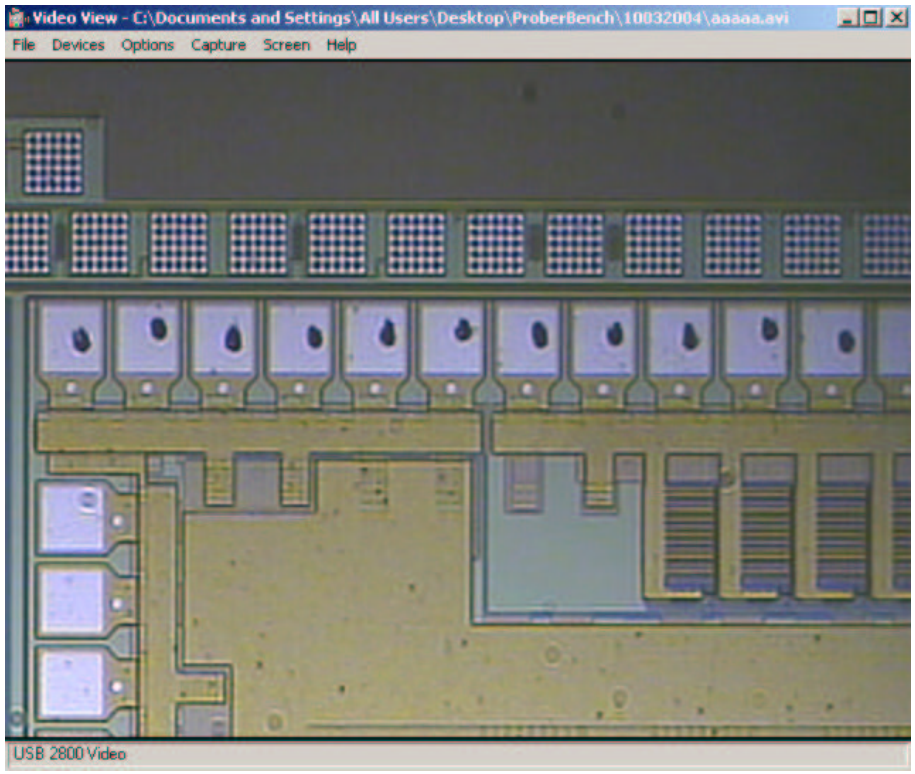
- An example of problem wafer map(ATA4I5T:9th)



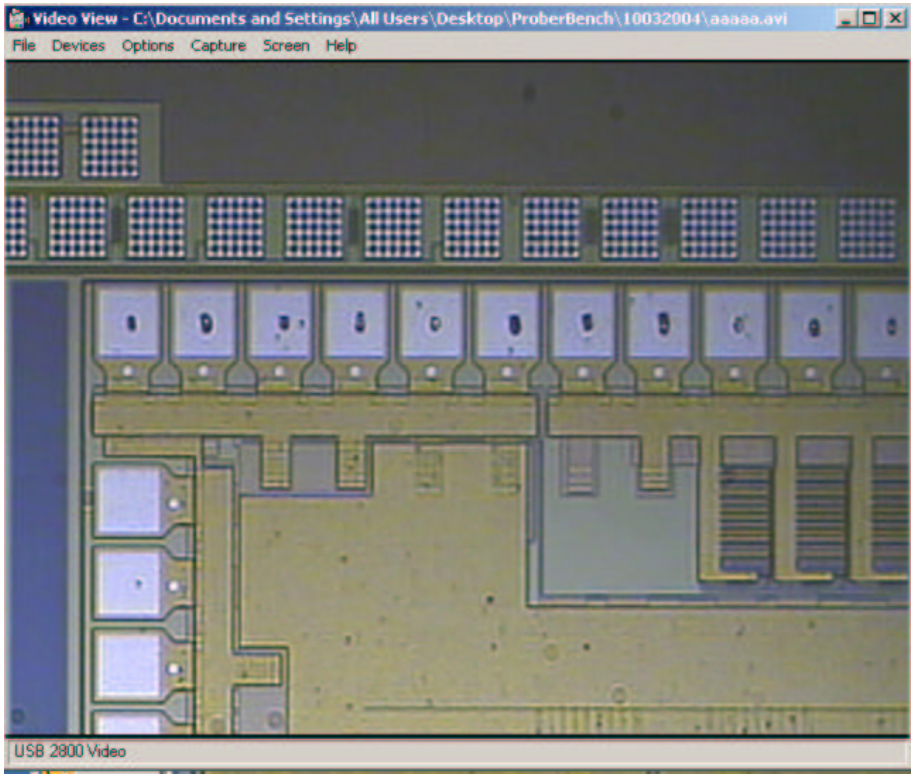
Wafer name	Recovered chips	Recovered / Problem
ATA4I5T	8	27.5%

- What is the couse?
  - ☆ These wafers might have a production error?
  - ☆ Probe neeldes on the probe card became bad?

- No resharpened tips



- Resharpened tips



↓

Now these couses are investigated by me and ALICE group.

5. Summary

☆ We get the yeild rate as the following.

Class 1	31.3%	374 chips
Class 2	10.1%	120 chips
Class 3	57.6%	698 chips

☆ At present we have 374 Class 1 chips, and need 226 chips more.

☆ We will be finished probing 15 and half wafers by the end of this month.

☆ We expect that in order to get 600 Class 1 chips, it is neccesary to prepare 5 wafers at least.

☆ 28 out of 77 chips were recovered by increasing Vdd_Analog in total.

☆ A ladder should be constructed with chips which are driven with same Vdd_Analog. Or these chips should be used as single assemblies.

☆ We will cross-check problem chips by a reshepened needles.

☆ The prober at CERN will be brought to RIKEN in the beginning of February in 2005.

☆ We will continue probing new wafers and ladders after bringing the prober.